AMENDMENT UNDER 37 C.F.R. 1.116 – EXPEDITED PROCEDURE

Serial Number: 10/646,478

Filing Date: August 22, 2003 Title: STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

Assignee: Intel Corporation

IN THE DRAWINGS

Corrected drawings are supplied herewith, each labeled as "REPLACEMENT SHEET".

Applicant has provided corrected FIGS. that correct the cross-hatching according to the specification.

AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 10/646,478 Filing Date: August 22, 2003

Title: STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

Assignee: Intel Corporation

REMARKS

This paper responds to the Office Action mailed on June 29, 2005. Claims 22-39 are canceled and claims 40-58 are added such that claims 40-58 are now pending in this application.

Interview Summary

Applicant thanks Examiner Ishwar B. Patel for the courtesy of a telephone interview on July 20, 2005 with Applicant's representative Andrew R. Peret. Examiner Patel discussed the new claims and the cited references with Applicant's attorney.

Applicant's attorney and Examiner Patel agreed that the pending rejections appear to be overcome by the new claims. Examiner Patel indicated that further searching and reconsideration would be required.

Objection to the Claims

Claims 22-39 were objected to due to informalities. Applicant has canceled claims 22-39 such that the pending objection is moot.

§102 Rejections of the Claims

Claims 22-25 and 28 were rejected under 35 USC § 102(e) as being anticipated by Carpenter et al. (U.S. 6,810,583).

Claims 31-34 and 37 were also rejected under 35 USC § 102(e) as being anticipated by Carpenter et al.

Applicant has canceled claims 22-25, 28, 31-34 and 37 such that the pending § 102(e) rejections are moot.

§103 Rejections of the Claims

Claims 26, 27, 35 and 36 were rejected under 35 USC § 103(a) as being unpatentable over Carpenter et al.

Claims 29, 30, 38 and 39 were also rejected under 35 USC § 103(a) as being unpatentable over Carpenter et al. and further in view of Uchikawa et al. (U.S. 6,531,661), Asai et al. (U.S. 6,534,723) and Kumar (U.S. 5,227,013).

AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 10/646,478 Filing Date: August 22, 2003

Title: STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

Assignee: Intel Corporation

Applicant has canceled claims 26, 27, 35, 36, 38 and 39 such that the pending § 103(a) rejections are moot.

Reservation of Right to File Continuation or Divisional Applications

Applicant respectfully traverses the rejection listed above and reserves the right to reintroduce any claims their original form in one or more continuation or divisional applications at a later date.

Reservation of Right to Swear Behind References

Applicant reserves the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

New Claims 40-58

Support for new claims 40-58 is found in the specification and the enclosed drawings. Applicant notes that the Carpenter et al. reference does not appear to include (among other items):

"a second conductive layer between the second dielectric layer and the third dielectric layer, the second conductive layer including a first skip via that extends through the first and second dielectric layers" and "a third conductive layer on the third dielectric layer, the third conductive layer including a second via that extends through the third dielectric layer, the second via and the first skip via being stacked on top of one another" as recited in claim 40;

"a second conductive layer between the second and third dielectric layers, the second conductive layer including a first skip via that extends through the first and second dielectric layers" and "a fourth conductive layer on the fourth dielectric layer, the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another" as recited in claim 47; or

Serial Number: 10/646,478 Filing Date: August 22, 2003

Title: STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

Assignee: Intel Corporation

"a sixth conductive layer on the sixth dielectric layer, the sixth conductive layer including a third skip via that extends through the fifth and sixth dielectric layers" as recited in claim 54.

Applicant respectfully directs the Examiner's attention to the FIGS. in Carpenter et al. which illustrate that the metallizations (e.g., metallizations 31, 28 and 29) in Carpenter et al. are separate from the vias (e.g., vias 36, 24, 26) such that the metallizations do not include vias. Applicant notes that none of metallizations disclosed in Carpenter et al. appear to include vias.

Allowance of claims 40-58 is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Andrew Peret at 262-646-7009, or the below-signed attorney at 612-349-9592, to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

DAISUKE KAWAGOE

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Attorneys for Intel Corporation

P.O. Box 2938

Minneapolis, Minnesota 55402

(612) 349-9592

Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 26 day of August 2005.

Signature